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BEFORE THE BOARD OF PATENT APPEALS

AND INTERFERENCES

Paper No. 31

Application Number: 08/984,560

Filing Date: 12/03/97

Appellant(s): Mailloux et al.

Timothy B. Clise

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 4/17/2003.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct. However, the amendment in the brief filed on 4/17/03 has not been entered.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The appellant's statement in the brief that all claims are to be taken independently of each other and each stands alone for the purpose of this appeal is not agreed with because Applicant has not provided independent argument for each of the claims that allegedly stand alone for the purposes of this appeal, see 37 CFR 1.192(c)(7)(8) and MPEP § 1206. Applicant provides ten arguments that seemingly apply to all of the claims, therefore, the Examiner believes that grouping of claims into ten groups is appropriate:

Group I, (claims 11, 59-62, 65, 68, 70, & 71), switching circuitry for switching between a first/pipelined pathway and a second/burst path way depending on which of a patternless/pipelined, addressing scheme and a patterned/burst addressing scheme is selected;

Group II, (claims 13 & 63), a temporary buffer for providing an external address;

Group III, (claims 19, 67 & 69), a multiplexed device;

Group VI, (claim 20), random column address access as part of the pipelined architecture;

Group V, (claims 64, 17, 18, & 66), pipelined and burst EDO patterns;

Group VI, (claim 12), an asynchronous device;

Group VII, (claim 14), a decoder;

Group VIII, (claim 15), a counter;

Group IX, (claim 16), internal address is provided to the temporary device through the switching circuit; and

Group X, (claim 21), an interleaved address access and a liner address access.

Merely pointing out differences in what the claim cover is not an argument as to why the claims are separately patentable.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

5,610,864	Manning	3-1997

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 11-21 and 59-71 were rejected under 35 USC 102(b) as being anticipated by *Manning*, U.S. Patent 5,610,864, however, Examiner acknowledges that there is a typo error on the last office action, therefore 102 (b) should be changed to 102 (e), since the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who

has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

This rejection is set forth in prior Office Action, Paper No. 28.

(11) Response to Argument

Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

In response to applicant's argument that the rejection should be characterized under 35 U.S.C. 102 (e), Examiner acknowledges that there is a typo error on the last office action, therefore, 102 (b) should be changed to 102 (e) in the final rejection, since the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

In response to applicant's argument at the bottom of page 4 in the Appeal Brief that the cited reference does not disclose "switching circuitry for switching between a first pathway and a

second path way depending on which of a patternless addressing scheme and a patterned addressing scheme is selected" has been fully considered but it is not persuasive.

Manning (864) discloses switching circuitry for switching between a first pathway and a second path way (col 6 lines 14-16 & Fig. 1 and col. 7 lines 44-55 in Manning) depending on which of a patternless addressing scheme (col. 5 lines 43-50) and a patterned addressing scheme is selected (col 6 lines 14-16 & Fig. 1 and col. 7 lines 44-55 in Manning). Specifically, Manning discloses detailed switching operation in col. 7 lines 50-54 "A more complex memory device may provide additional modes of operation such as switching between fast page mode, EDO page mode, static column mode and burst operation through the use of various combinations of /WE and /OE at /RAS falling time" and col. 6 lines 14-19, " The memory device of FIG. 1 may include the option of switching between burst EDO and standard EDO modes of operation. In this case, the write enable signal /WE 36 is used at the row address latch time (/RAS falling, /CAS high) to determine whether memory accesses for that row are burst or page mode cycles". Furthermore, "The current invention include a pipelined architecture where memory accesses are performed sequentially" (col. 5 lines 43-49 in Manning) and "switching between burst EDO mode and standard EDO mode" (see col 6 lines 14-16 & Fig. 1 and col. 7 lines 44-55 in Manning), therefore, Manning discloses the claimed limitation. In other words, in order to work in *a standard EDO memory including a pipelined architecture, one has to select a pipelined mode* if one is in a burst mode. Also it is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory

read, memory write, memory address input, memory data input or memory data output to be processed simultaneously. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area. Therefore, Manning (864) discloses switching circuitry for switching between a first pathway and a second path way (col 6 lines 14-16 & Fig. 1 and col. 7 lines 44-55 in Manning) depending on which of a patternless addressing scheme (col. 5 lines 43-50) and a patterned addressing scheme is selected (col 6 lines 14-16 & Fig. 1 and col. 7 lines 44-55 in Manning).

In response to applicant's argument at the top of page 7 in the Appeal Brief that only a burst EDO memory includes pipelined architecture has been fully considered but it is not persuasive.

Examiner disagrees with applicants because Manning discloses that "The current invention include a pipelined architecture where memory accesses are performed sequentially", col 5 lines 43-49. In other words, pipelined architecture can be used on standard EDO, fast page mode,

static column, and burst modes, (see col. 7 lines 50-54). Therefore, in order to work in a standard EDO memory includes pipelined architecture, one has to select a pipelined mode.

A. Response to Argument of Claim Group I, (claims 11, 59-62, 65, 68, 70, & 71)

1. Appellants' argument at the bottom of page 4 an the top of page 6 in the Appeal Brief that the cited reference does not disclose "switching circuitry for switching between a first/pipelined pathway and a second/burst path way depending on which of a patternless/pipelined, addressing scheme and a patterned/burst addressing scheme is selected" has been fully considered but it is not persuasive.

Manning (864) discloses switching circuitry for switching circuitry for switching between a first/pipelined pathway and a second/burst path way (col 6 lines 14-16 & Fig. 1 and col. 7 lines 44-55 in Manning) depending on which of a patternless/pipelined addressing scheme (col. 5 lines 43-50) and a patterned/burst addressing scheme is selected (col 6 lines 14-16 & Fig. 1 and col. 7 lines 44-55 in Manning). Specifically, Manning discloses detailed switching operation in col. 7 lines 50-54 "A more complex memory device may provide additional modes of operation such as switching between fast page mode, EDO page mode, static column mode and burst operation through the use of various combinations of /WE and /OE at /RAS falling time" and col. 6 lines 14-19, " The memory device of FIG. 1 may include the option of switching between burst EDO and standard EDO modes of operation. In this case, the write enable signal /WE 36 is used at the row address latch time (/RAS falling, /CAS high) to determine whether memory accesses for that

row are burst or page mode cycles". Furthermore, "The current invention include a pipelined architecture where memory accesses are performed sequentially" (col. 5 lines 43-49 in Manning) and "switching between burst EDO mode and standard EDO mode" (see col 6 lines 14-16 & Fig. 1 and col. 7 lines 44-55 in Manning) read on this limitation. In other words, in order to work in a standard EDO memory including a pipelined architecture, one has to select a pipelined mode if one is in a burst mode. Also it is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area. Therefore, Manning (864) discloses switching circuitry for switching between a first pathway and a second path way (col 6 lines 14-16 & Fig. 1 and col. 7 lines 44-55 in Manning) depending on which of a patternless addressing scheme (col. 5 lines 43-50) and a patterned addressing scheme is selected (col 6 lines 14-16 & Fig. 1 and col. 7 lines 44-55 in Manning).

B. Response to Argument of Claim Group II, (claims 13 & 63)

1. Appellants' argument at the bottom of page 5 in the Appeal Brief that the cited reference does not disclose "a temporary buffer for providing an external address" has been fully considered but it is not persuasive.

Manning (864) discloses a temporary buffer for providing an external address (Fig. 1 Ref. 26 and 18 and col. 6 line 28 and col. 4 lines 23-25).

C. Response to Argument of Claim Group III, (claims 19, 67 & 69)

1. Appellants' argument at the bottom of page 5 in the Appeal Brief that the cited reference does not disclose "a multiplexed device" has been fully considered but it is not persuasive.

Manning (864) discloses a multiplexed device (Fig. 1 Ref. 26, controlling the column address counter/latch between burst and pipelined modes reads on this limitation, because during the burst operation, the address is incremented internal to the device eliminating the need for external address lines to switch at high frequencies, col. 3 lines 19-21 and col. 5 lines 50-57, however, during the pipelined operation, each column address is provided one access per cycle, col. 5 line 43-50. In other words, during the burst mode, an internal counter/latch path is selected however, during the pipelined mode, an external counter/latch path is selected, see also col. 6 lines 26-34).

D. Response to Argument of Claim Group VI, (claim 20)

1. Appellants' argument at the top of page 6 in the Appeal Brief that the cited reference does not disclose "random column address access as part of the pipelined architecture" has been fully considered but it is not persuasive.

Manning (864) discloses random column address access as part of the pipelined architecture (col. 5 lines 42-50, since a new (random) address is provided to an address input terminal every cycle during a pipelined mode operation). In other words, accessing a non burst memory such as a standard EDO memory including a pipelined architecture, a new external address should be provided to an input address terminal every memory access cycle in order to take an advantage of the pipelined architecture since the pipelined architecture effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe.

E. Response to Argument of Claim Group V, (claims 64, 17, 18, & 66)

1. Appellants' argument at the bottom of page 8 in the Appeal Brief that the cited reference does not disclose "pipelined and burst EDO patterns" has been fully considered but it is not persuasive.

Manning (864) discloses pipelined and burst EDO patterns. "The current invention include a pipelined architecture where memory accesses are performed sequentially" (col. 5 lines 43-49 in Manning) and "switching between burst EDO mode and standard EDO mode" (see col 6 lines 14-16 & Fig. 1 and col. 7 lines 44-55 in Manning) read on this limitation.

F. Response to Argument of Claim Group VI, (claim 12)

Manning (864) discloses an asynchronous device (the standard EDO constitutes asynchronous memory, col. 6 lines 14-16, since the standard EDO does not require a clock or strobe signal, see Fig. 1).

G. Response to Argument of Claim Group VII, (claim 14)

Manning (864) discloses a decoder (Fig. 1 Ref. 30 and col. 4 lines 23-26).

H. Response to Argument of Claim Group VIII, (claim 15)

Manning (864) discloses a counter (Fig. 1 Ref. 26 and col. 3 lines 20-23).

I. Response to Argument of Claim Group IX, (claim 16)

Manning (864) discloses internal address is provided to the temporary device through the switching circuit (col. 3 lines 20-23 and Fig. 1).

J. Response to Argument of Claim Group X, (claim 21)

Manning (864) discloses an interleaved address access and a liner address access (col. 4 lines 56-57).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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May 28, 2003

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